**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**

**HYDERABAD CAMPUS**

**SECOND SEMESTER 2020- 2021**

**COURSE HANDOUT (PART II)**

Date: 16/01/2021

In addition to Part I (General Handout for all courses appended to the timetable) this portion gives further specific details regarding the course.

*Course No* : **CS F342**

*Course Title* : **Computer Architecture**

*Instructor-in-charge* : **Chetan Kumar V**

*Instructors*  : **Chetan Kumar V, Sharvani Gadgil (PhD Scholar), P N Sidhartha (PhD Scholar)**

*Email* : [chetan@hyderabad.bits-pilani.ac.in](mailto:chetan@hyderabad.bits-pilani.ac.in)

1. **Scope and Objective:**

This course aims at introducing the concept of computer architecture. It involves design aspects, and deals with the current trends in computing architecture. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will also be discussed.

Processor performance criteria, performance bench-marks, arithmetic circuits, CPU design - instruction set architecture, instruction execution, Single and Multicycle implementation, Pipeline design, Hazards, methods of overcoming hazards, Branch prediction, Memory subsystems including cache optimization, Instruction level Parallelism

1. **Learning Outcome:**

* Understand various factors affecting CPU (e.g. CPU Performance, Power Consumption etc.)
* Understand the fundamentals of instruction set architectures and their relationship to the CPU design.
* Understand the principles behind implementation of a basic MIPS processor.
* Understand the operation of pipelined CPUs including pipeline hazards and different ways to solve them.
* Understand the principles of memory organization, Caches and Virtual memory.
* Understand the basic principles of advanced pipelined processors and Multi-core processors.
* Design and emulate a single cycle or pipelined CPU by given specifications using Verilog Hardware Description Language (HDL).

1. **Text Book:**

**(T1)** Patterson, D.A. & J.L. Hennessy, Computer Organization and Design, Elsevier, 4th ed., 2009.

1. **Reference Books:**

(R1) Patterson, D.A. & J.L. Hennessy Computer Architecture: A Quantitative Approach, 5th Edition, 2012

(R2)William Stallings, *Computer Organisation & Architecture,* Pearson, 8th ed., 2010.

(R3) Hamacher et. al, *Computer Organisation*, McGraw Hill, 5th ed., 2002.

(R4) Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson Education, Asia, 2003.

1. **Course Plan:**

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| --- | --- | --- | --- |
| **Lecture No.** | **Learning objectives** | **Topics to be covered** | **Chapter in the Text Book** |
| **1** | Introduction | Introduction to the course | **1.1-1.3** |
| **2-4** | CPU Performance and its factors, Power limit and evolution of CPU | Current Trends in technology, power, Performance, Amdahl’s law, Problems | **1.4-1.6** |
| **5-10** | RISC Architecture & Instruction Set | Classification of ISA, RISC Instructions and encoding, Problems | **2.1-2.10, 2.16** |
| **11** | Data path Design | RISC Processor data path Implementation | **4.1-4.4** |
| **12** | Control Hardware | RISC Processor control path Implementation | **Appendix-D and Class Notes** |
| **13-15** | Pipelining Overview, Pipelined Datapath and Control | Pipelining concepts, introduction to Data and Control Hazards, Pipeline Implementation, Problems | **4.5-4.6** |
| **16-19** | Data Hazards, Control hazards, Branch Prediction | Forwarding, stall condition implementation, Problems | **4.7-4.9** |
| **Reading Assignment** | Computer Arithmetic | Implementation of Basic arithmetic operations, Problems | **3.1-3.4** |
| **20-21** | Floating Point Arithmetic | Implementation of Floating-point arithmetic operations, Problems | **3.5-3.7** |
| **22-23** | Memory Organization Introduction | Organization of memory | **5.1 and Class Notes** |
| **24-29** | Basics of cache, Measuring and improving performance of Cache | Basics of cache, Direct mapped, Fully associative, cache performance, Problems | **5.2-5.3** |
| **30-32** | Virtual Memory | Virtual Memory, Page table, TLB, Problems | **5.4** |
| **33-35** | Advanced Topics: Advanced Instruction Level Parallelism | Overview, ILP based processor designs | **4.10, Class Notes** |
| **36-39** | Modern Processors: Special Purpose, Multicore | Multicore processor challenges, Cache Coherence | **7.1-7.6, Class Notes** |
| **40-41** | Storage and IO Organization, Interfacing of IO devices | Buses and other connection between processor, memory and I/O devices, Interfacing of IO devices | **6.1-6.2**  **6.5-6.6** |
| **Reading Assignment** | Storage Concepts | Storage Concepts | **6.3-6.4, 6.9** |

1. **Evaluation Scheme:**

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| --- | --- | --- | --- | --- |
| **Component** | **Duration** | **Weightage (%)** | **Date & Time** | **Nature of Component** |
| Mid-Sem Examination | 90 Min | 50 (25%) | 05/03 9.00 -10.3AM | OB |
| Weekly Lab Experiments (Reports) | NA | 20(10%) | Continuous | OB |
| Lab Exam | 60 Min | 20 (10%) | To Be Announced |  |
| Assignments | NA | 30(15%) | To Be Announced | OB |
| Comprehensive Examination | 120 Min | 80 (40%) | 12/05 FN | OB |

1. **Self-Study/Reading Assignment:** “Course will have some self-study components which will be announced periodically”
2. **Chamber Consultation Hours:** To be announced in the class
3. **Notices:** Notices regarding the course will be put up on CMS.
4. **Makeup Policy:** No makeup exam allowed without prior permission.
5. **Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

Instructor - in - charge

CS F342